XA-9574
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Hideki YASUOKA et al.

Serial No.: 09/989,061 Group Art Unit: 2812

Filed: November 21, 2001 Examiner: J. Kennedy

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD OF MANUFACTURING THE SAME

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. § 1.56, and without any assertion as to materiality or prior art effect, the document listed on the attached Form PTO-1449 is hereby cited.

The document on the attached List is a counterpart of Japanese Patent Application Laid-Open No. Hei 11(1999)-177047 which was cited in the specification, on page 1, and its relevance is indicated therein.

A check for $180.00 is attached to cover the fee set forth in 37 C.F.R. § 1.17(p).

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to

credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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